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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/774,536 | 02/10/2004 | Yuichi Sato | 204552016501 | 3216 |

7590 02/07/2005

Barry E. Bretschneider
Morrison & Foerster LLP
Suite 300
1650 Tysons Boulevard
McLean, VA 22102

| EXAMINER | |
|---|---|
| WILLE, DOUGLAS A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/774,536 | SATO, YUICHI | |
| | Examiner | Art Unit | |
| | Douglas A. Wille | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0204*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. Claims 1, 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art and Hu et al.

2. With respect to claim 1, Applicant's admitted prior art, Figure 9, shows an SRAM comprised of CMOS devices. Hu et al. show a DTMOS device (see Figure 7 and column 1, line 8 et seq.) that has the n-well deeper than the p-well and that can be used in CMOS circuitry for the advantages shown (column 2, line 46). It would have been obvious to modify the basic device to include the DTMOS device shown by Hu et al. for the advantages shown. Note that the gates are electrically connected.

3. With respect to claim 2, note that the gates of the devices are connected to a power supply and therefore, so are the channel forming regions.

4. With respect to claim 4, Hu et al. show a DTMOS device (see Figure 7 and column 1, line 8 et seq.) that has the n-well deeper than the p-well.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art and Hu et al. and further in view of Tsui et al.

6. Tsui et al. show the use of dual thickness gate oxides with thinner gate oxides used for low voltage devices (column 1, line 14). Since DTMOS devices use lower voltages it would have been obvious to use thinner oxides for the lower voltage devices and to use normal gate oxides for other devices.

7. Claims 5, 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art and Hu et al. and further in view of Hodges et al.

8. With respect to claim 5, Hodges et al. show the formation of peripheral circuits for a memory device that use MOS structures (see page 368 and 369) and it would be obvious to use the DTMOS devices for these structures for the advantages shown.

9. With respect to claim 6, bit lines are shown.

10. With respect to claim 9, Hu et al. show a DTMOS device (see Figure 7 and column 1, line 8 et seq.) that has the n-well deeper than the p-well.

11. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art and Hu et al. and further in view of Hodges.

12. Hodges shows a SRAM which uses resistors as an alternative SRAM to that shown in Applicant's admitted prior art (see cover Figure) and it would be obvious to use that circuit as a design choice and to use the DTMOS devices for the advantages shown.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas A. Wille whose telephone number is (571) 272-1721. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Douglas A. Wille
Patent Examiner